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EXAMINER	
BAUM, RONALD	

ART UNIT	PAPER NUMBER
2135	7

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Please find below and/or attached an Office communication concerning this application or proceeding.

PRG

Office Action Summary	Application No.	Applicant(s)	
	09/675,113	HALE ET AL.	
	Examiner	Art Unit	
	Ronald Baum	2135	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-33 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-33 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3,5,6 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-33 are pending for examination.

2. Claims 1-33 are rejected.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1- 33 are rejected under 35 U.S.C. 102(e) as being anticipated by Davis et al, U.S. Patent 6,401,208 B2.

4. As per claim 1; "Embodied in a memory component, a digitally signed image comprising: a post-relocation image being an image of a software module altered by a symmetrical relocation function upon loading of the image into the memory component; and a digital signature based on the image [abstract, col. 3, col. 4,lines 41-59, lines 25-40, col. 5,lines 9-43, whereas the phrase "symmetrical relocation *function*" taken in the broadest meaning of the words is the Davis et al BIOS software (firmware) module segments distributed as shown in figure 1, across various peripheral blocks (i.e., different, relocated by PC motherboard slot connectors). Further, as per the inherent addressing of peripherals according to the "board slot" location within the motherboard (i.e., PCI) bus structure, such location addressing is inherent relocation (col. 3, lines 14-24).]. ";

And further as per claim 24; ""An electronic device comprising [This claim is the embodied in software of claim 1, with a processor, and is the said embodied software is rejected for the same reasons provided for the claim 1 rejection above, while the teachings of Davis et al clearly include a processor (abstract, figures 1-5 and accompanying descriptions)]: a processor; and a non-volatile memory component in communication with the processor, the non-volatile memory component includes including a post-relocation image being an image of a software module altered by a symmetrical relocation function upon loading of the image into the memory component, and a digital signature based on the image.".

5. Claim 2 ***additionally recites*** the limitations that; "The digitally signed image of claim 1, wherein the digital signature is a hash value of the image digitally signed by a private key of a selected signatory. ". The teachings of Davis et al (col. 2,lines 44-col. 3,line 5, col. 8,lines 55-63) suggest such limitations;

6. Claim 3 ***additionally recites*** the limitations that; "The digitally signed image of claim 1 further comprising information for use by the symmetrical relocation function to convert the image into the relocation image. ". The teachings of Davis et al (col. 5,lines 9-43, again, whereas the phrase "symmetrical relocation *function*" taken in the broadest meaning of the words is the Davis et al BIOS software (firmware) module segments distributed as shown in figure 1, across various peripheral blocks (i.e., different, relocated by PC motherboard slot connectors). Further, as per the inherent addressing by the crypto device addressing (i.e., read/ write access) of peripherals according to the "board slot" location within the motherboard (i.e., PCI) bus structure, such location addressing is inherent relocation (col. 3, lines 14-24).) suggest such limitations;

And further as per claim 25; "The electronic device of claim 24 [This claim is the embodied in software of claim 3, with a processor, and is the said embodied software is rejected for the same reasons provided for the claim 3 rejection above, while the teachings of Davis et al clearly include a processor (abstract, figures 1-5 and accompanying descriptions)], wherein the non-volatile memory component further includes information for use by the symmetrical relocation function to convert the image into the post-relocation image.".

7. Claim 4 ***additionally recites*** the limitations that; "The digitally signed image of claim 3, wherein the information includes offsets for routines within the software module.". The teachings of Davis et al (col. 5,lines 9-43, again, whereas the phrase "symmetrical relocation *function*" taken in the broadest meaning of the words is the Davis et al BIOS software (firmware) module segments distributed as shown in figure 1, across various peripheral blocks (i.e., different, relocated by PC motherboard slot connectors). Further, as per the inherent addressing by the crypto device addressing (i.e., read/ write access) of peripherals according to the "board slot" location within the motherboard (i.e., PCI) bus structure, such location addressing is inherent relocation (col. 3, lines 14-24), where access is in the form of vectors (i.e., a table of offsets thereof) pointing to the execution starting points of the specific code routines (i.e., interrupt service routines, drivers, etc.).) suggest such limitations;

And further as per claim 26; "The electronic device of claim 25 [This claim is the embodied in software of claim 4, with a processor, and is the said embodied software is rejected for the same reasons provided for the claim 4 rejection above, while the teachings of Davis et al clearly include a processor (abstract, figures 1-5 and accompanying descriptions)], wherein the information placed within the non-volatile memory component includes offsets from a starting

address of the image of the software module to a segment of information within the software module.".

8. Claim 5 ***additionally recites*** the limitations that; "The digitally signed image of claim 4, wherein the offsets are generated when the software module is compiled.". The teachings of Davis et al (col. 5,lines 9-43, again, whereas the phrase "symmetrical relocation *function*" taken in the broadest meaning of the words is the Davis et al BIOS software (firmware) module segments distributed as shown in figure 1, across various peripheral blocks (i.e., different, relocated by PC motherboard slot connectors). Further, as per the inherent addressing by the crypto device addressing (i.e., read/ write access) of peripherals according to the "board slot" location within the motherboard (i.e., PCI) bus structure, such location addressing is inherent relocation (col. 3, lines 14-24), where access is in the form of vectors (i.e., a table of offsets thereof) pointing to the execution starting points of the specific code routines (i.e., interrupt service routines, drivers, etc.) that are clearly *generated at the time of manufacture.*)suggest such limitations.

9. As per claim 6; "Embodied in a memory component, a digitally signed image comprising: a Bound & Relocated Import Table (BRIT); an import table; an export table; an image of a software module; and a digital signature based on the import table, the export table and the image [abstract, col. 3, col. 4,lines 41-59, lines 25-40, col. 5,lines 9-43, whereas the phrases "Bound & Relocated Import Table (BRIT); an import table; an export table" taken in the broadest meaning of the words is the software (firmware) module segments *inherently linked in the post compiled* state, distributed as shown in figure 1, across various peripheral blocks (i.e., different, relocated by PC motherboard slot connectors). Further, this is claim 1 with the

limitation of more explicitly describing the inherent linking and address resolution of 'inter' and 'intra' software modules, post compilation, (i.e., the inherently specific function of the linker in the software development design), as per the teachings of the Davis et al invention, and is rejected on the same basis as claim 1.].";

And further as per claim 27; "An electronic device comprising [This claim is the embodied in software of claim 6, with a processor, and is the said embodied software is rejected for the same reasons provided for the claim 6 rejection above, while the teachings of Davis et al clearly include a processor (abstract, figures 1-5 and accompanying descriptions)]: a processor; and a memory in communication with the processor, the memory being loaded with a Bound & Relocated Import Table (BRIT), an import table, an export table, an image of a software module, and a digital signature based on the import table, the export table and the image.".

10. Claim 7 ***additionally recites*** the limitations that; "The digitally signed image of claim 6, wherein the import table comprises a plurality of entries, each entry includes an identifier that indicates what segment of information contained in another digitally signed image is required by the image.". This is a claim 6 limitation of more explicitly describing the inherent linking, address, and *symbol* resolution of 'inter' and 'intra' software modules, post compilation, (i.e., the inherently specific function of the linker in the software development design), as per the teachings of the Davis et al invention, and is rejected on the same basis as claim 6;

And further as per claim 28; "The electronic device of claim 27 [This claim is the embodied in software of claim 7, with a processor, and is the said embodied software is rejected for the same reasons provided for the claim 7 rejection above, while the teachings of Davis et al clearly include a processor (abstract, figures 1-5 and accompanying descriptions)], wherein the

import table loaded within the memory comprises a plurality of entries, each entry includes an identifier that indicates what segment of information contained in another digitally signed image is required by the image.".

11. Claim 8 ***additionally recites*** the limitations that; "The digitally signed image of claim 7, wherein the identifier includes a unique sequence of byte values.". This is a claim 7 limitation of more explicitly describing the inherent linking, address, and *symbol* resolution of 'inter' and 'intra' software modules, post compilation, (i.e., the inherently specific function of the linker in the software development design), whereas, it is also inherent that such symbols in the multi-segment module(s) would have a unique ID (i.e., sequence of bytes, inclusive of the representation of said bytes as alphanumeric or "binary", hexadecimal, etc.) for the compiling and linking process to work correctly, as per the teachings of the Davis et al invention, and is rejected on the same basis as claim 7;

And further as per claim 29; "The electronic device of claim 28 [This claim is the embodied in software of claim 8, with a processor, and is the said embodied software is rejected for the same reasons provided for the claim 8 rejection above, while the teachings of Davis et al clearly include a processor (abstract, figures 1-5 and accompanying descriptions)], wherein the identifier associated with a particular entry include a unique sequence of byte values.".

12. Claim 9 ***additionally recites*** the limitations that; "The digitally signed image of claim 7, wherein the identifier includes a unique sequence of alphanumeric characters.". This is a claim 7 limitation of more explicitly describing the inherent linking, address, and *symbol* resolution of 'inter' and 'intra' software modules, post compilation, (i.e., the inherently specific function of the linker in the software development design), whereas, it is also inherent that such symbols in

the multi-segment module(s) would have a unique ID (i.e., sequence of bytes, inclusive of the representation of said bytes as alphanumeric or "binary", hexadecimal, etc.) for the compiling and linking process to work correctly, as per the teachings of the Davis et al invention, and is rejected on the same basis as claim 7.

13. Claim 10 ***additionally recites*** the limitations that; "The digitally signed image of claim 7, wherein each entry of the import table further includes an offset to a corresponding entry of the BRIT.". This is a claim 7 limitation of more explicitly describing the inherent linking, address, and *symbol* resolution of 'inter' and 'intra' software modules, for both *calling* and *called* aspects (i.e., import and export in the form of a table(s)) of function reference, post compilation, (i.e., the inherently specific function of the linker in the software development design); whereas, it is also inherent that such symbols in the multi-segment module(s) would have a unique ID (i.e., sequence of bytes, inclusive of the representation of said bytes as alphanumeric or "binary", hexadecimal, etc.) for the compiling and linking process to work correctly, as per the teachings of the Davis et al invention, and is rejected on the same basis as claim 7.

14. Claim 11 ***additionally recites*** the limitations that; "The digitally signed image of claim 6, wherein the export table includes a plurality of entries forming a listing of segments of information contained in the image, a selected entry of the plurality of entries includes an identifier of a segment of information associated with the segments of information.". This is a claim 6 limitation of more explicitly describing the inherent linking, address, and *symbol* resolution of 'inter' and 'intra' software modules, for both *calling* and *called* aspects (i.e., import and *export* in the form of a table(s)) of function reference, post compilation, (i.e., the inherently specific function of the linker in the software development design); whereas, it is also inherent

that such symbols in the multi-segment module(s) would have a unique ID (i.e., sequence of bytes, inclusive of the representation of said bytes as alphanumeric or "binary", hexadecimal, etc.) for the compiling and linking process to work correctly, as per the teachings of the Davis et al invention, and is rejected on the same basis as claim 6;

And further as per claim 30; "The electronic device of claim 27 [This claim is the embodied in software of claim 11, with a processor, and is the said embodied software is rejected for the same reasons provided for the claim 11 rejection above, while the teachings of Davis et al clearly include a processor (abstract, figures 1-5 and accompanying descriptions)], wherein the export table includes a plurality of entries forming a listing of segments of information contained in the image, a selected entry of the plurality of entries includes an identifier of a segment of information associated with the segments of information. ".

15. Claim 12 ***additionally recites*** the limitations that; "The digitally signed image of claim 11, wherein the selected entry further includes a second offset being an offset from a starting address of the digitally signed image to an address location of the segment of information. ". This is a claim 11 limitation of more explicitly describing the inherent linking, address, and *symbol* resolution of 'inter' and 'intra' software modules, for both *calling* and *called* aspects (i.e., import and *export* in the form of a table(s), both *direct and indirect* (1^{st}, 2^{nd}, etc., level of offsets)) of function reference, post compilation, (i.e., the inherently specific function of the linker in the software development design); whereas, it is also inherent that such symbols in the multi-segment module(s) would have a unique ID (i.e., sequence of bytes, inclusive of the representation of said bytes as alphanumeric or "binary", hexadecimal, etc.) for the compiling

and linking process to work correctly, as per the teachings of the Davis et al invention, and is rejected on the same basis as claim 11.

16. As per claim 13; "A method comprising [This claim is a method of the apparatus (device) claim 1, and is rejected for the same reasons provided for the claim 1 rejection above]: reconverting a post-relocation image of a digitally signed image back to a pre-relocation image, the pre-relocation image being art image of a software module prior to be altered by a symmetrical relocation function; conducting a hash operation on the reconverted, pre-relocation image to produce a reconverted hash value; recovering a hash value from a digital signature contained in the digitally signed image, the hash value is based on the image of the software module; and comparing the hash value to the reconverted hash value. [abstract, col. 3, col. 4,lines 41-59, lines 25-40, col. 5,lines 9-43, whereas the phrase "symmetrical relocation *function*" taken in the broadest meaning of the words is the Davis et al BIOS software (firmware) module segments distributed as shown in figure 1, across various peripheral blocks (i.e., different, relocated by PC motherboard slot connectors). Further, as per the inherent addressing of peripherals according to the "board slot" location within the motherboard (i.e., PCI) bus structure, such location addressing is inherent relocation (col. 3, lines 14-24).]. Also, the authentication and verification functions of Davis correspond to the applicant's comparison of reconverted hash to image hash (signature), see figure 6B";

And further as per claim 31; "Embodied in a processor readable medium for execution by a processor, a software program [This claim is the embodied in software method of the method claim 13, and is rejected for the same reasons provided for the claim 13 rejection above] comprising a first software module to reconvert a post-relocation image of a digitally signed

image back to a pre-relocation image, the pre-relocation image being an image of a software module prior to be altered by a symmetrical relocation function; a second software module to conduct a hash operation on the reconverted, pre-relocation image to produce a reconverted hash value; a third software module to recover a hash value from a digital signature contained in the digitally signed image, the hash value is based on the image of the software module; and a fourth software module to compare the hash value to the reconverted hash value.".

17. Claim 14 ***additionally recites*** the limitations that; "The method of claim 13 further comprising: determining that an integrity of the post-relocation image remains intact if the hash value matches the reconverted hash value.". The teachings of Davis et al (figure 6B, the authentication and verification functions of Davis correspond to the applicant's comparison of reconverted hash to image hash (signature)) suggest such limitations;

And further as per claim 32; "The software program of claim 31 [This claim is the embodied in software method of the method claim 14, and is rejected for the same reasons provided for the claim 14 rejection above] further comprising: a fifth software module to determine that an integrity of the post-relocation image remains intact if the hash value matches the reconverted hash value. "

18. Claim 15 ***additionally recites*** the limitations that; "The method of claim 13 further comprising: determining that the post-relocation image has been modified beyond any modification caused by relocation when the hash value fails to match the reconverted hash value.". The teachings of Davis et al (figure 6B, the authentication and verification functions of Davis correspond to the applicant's comparison of reconverted hash to image hash (signature)) suggest such limitations.

And further as per claim 33; "The software program of claim 31 [This claim is the embodied in software method of the method claim 15, and is rejected for the same reasons provided for the claim 15 rejection above] further comprising a sixth software module to determine that the post-relocation image has been modified beyond any modifications caused by relocation when the hash value fails to match the reconverted hash value. "

19. Claim 16 ***additionally recites*** the limitations that; "The method of claim 13, wherein the hash operation is a one-way hash operation.". The teachings of Davis et al (col. 2,lines 44-col. 3,line 5, col. 6,lines 14-19,) suggest such limitations.

20. As per claim 17; "A method for generating a Bound & Relocated Import Table (BRIT) within an electronic device, comprising: (a) locating an import table for a first digitally signed image loaded within the electronic device, each entry of the import table including an identifier and a first offset; (b) accessing an identifier within a selected entry of the first digitally signed image; (c) determining whether the identifier matches an identifier within an export table of a second digitally signed image loaded within the electronic device, the identifier for the export table is stored with a corresponding second offset; and (d) upon determining that the identifier within the selected entry matches the identifier within the export table, producing an address by combining the second offset with a starting address of the second digitally signed image, and loading the identifier within the selected entry and the address into an entry of the BRIT. ". This is the claims 6-8,10,11 limitations of more explicitly describing the inherent part of the Davis et al *embedding of the software, post design/ generation*, with the inherent linking, address, and *symbol* resolution of 'inter' and 'intra' software modules, for both *calling* and *called* aspects (i.e., import and *export* in the form of a table(s)) of function reference, post compilation, (i.e., the

inherently specific function of the linker in the software development design); whereas, it is also inherent that such symbols in the multi-segment module(s) would have a unique ID (i.e., sequence of bytes, inclusive of the representation of said bytes as alphanumeric or "binary", hexadecimal, etc.) for the compiling and linking process to work correctly, as per the teachings of the Davis et al invention, and is rejected on the same basis as claims 6-8,10,11.

21. Claim 18 ***additionally recites*** the limitations that; "The method of claim 17 further comprising: repeating the operations of (a)-(d) for each remaining entry of the import table for loading resultant address and identifier pairs into different entries of the BRIT.". This is claim 17 where multiple segments, images, and software modules (developed, compiled, linked, and embedded) are involved, and it would be inherent in the Davis et al invention for multiple BIOS modules (i.e., figure 1 and accompanying description), to be involved as per the teachings of the Davis et al invention, and is rejected on the same basis as claim 17.

22. Claim 19 ***additionally recites*** the limitations that; "The method of claim 17, wherein the; producing of the address by combining the second offset with the starting address of the second digitally signed image comprises an arithmetic operation. ". This is claim 17 where multiple segments, images, and software modules (developed, compiled, linked, and embedded) are involved, and it would be inherent in the Davis et al invention for multiple BIOS modules (i.e., figure 1 and accompanying description) to have the linking process occur in software such that the offset symbol (label) and address resolution would use arithmetic operations, as per the inherent aspects of the teachings of the Davis et al invention, and is rejected on the same basis as claim 17.

23. Claim 20 ***additionally recites*** the limitations that; "The method of claim 17, wherein prior to locating an import table for the first digitally signed image, the method further comprises locating a plurality of digitally signed images loaded within the electronic device.". This is claim 17 where multiple segments, images, and software modules (developed, compiled, linked, and embedded) are involved, and it would be inherent in the Davis et al invention for multiple BIOS modules (i.e., figure 1 and accompanying description), to be involved as per the teachings of the Davis et al invention, and is rejected on the same basis as claim 17.

24. As per claim 21; "A method comprising: verifying an integrity of a plurality of digitally signed images loaded in an electronic device, the plurality of digitally signed images includes a first digitally signed image and a second digitally signed image; determining whether an identifier in an import table of the first digitally signed image matches an identifier in an export table of the second digitally signed image; and determining whether an entry of a Bound & Relocated Import Table (BRIT) corresponding to the identifier in the import table points to an address defined by the identifier in the export table. ". This is the claims 12,18-20 limitations of more explicitly describing the inherent part of the Davis et al *verifying and authentication of the software, post design/ generation*, for plural cases of verifiable software instances, with the inherent linking, address, and *symbol* resolution of 'inter' and 'intra' software modules, for both *calling* and *called* aspects (i.e., import and *export* in the form of a table(s)) of function reference, post compilation, (i.e., the inherently specific function of the linker in the software development design); whereas, it is also inherent that such symbols in the multi-segment module(s) would have a unique ID (i.e., sequence of bytes, inclusive of the representation of said bytes as alphanumeric or "binary", hexadecimal, etc.) for the compiling and linking process to work

correctly, as per the teachings of the Davis et al invention, and is rejected on the same basis as claims 12,18-20.

25. Claim 22 ***additionally recites*** the limitations that; "The method of claim 21, wherein the verifying the integrity of the plurality of digitally signed images includes performing a hash operation on the import table, the export table and an image of the first digitally signed image to produce a first resultant hash value; recovering a first hash value from a. digital signature contained in the first digitally signed image; and comparing the first hash value with the first resultant hash value.". The teachings of Davis et al (figure 6B, the authentication and verification functions of Davis correspond to the applicant's comparison of reconverted hash to image hash (signature)) suggest such limitations.

26. Claim 23 ***additionally recites*** the limitations that; "The method of claim 22, wherein the verifying the integrity of the plurality of digitally signed images further comprises performing a hash operation on an import table, an export table and an image of the second digitally signed image to produce a second resultant hash value; recovering a second hash value from a digital signature contained in the second digitally signed image; and comparing the second hash value with the second resultant hash value. ". The teachings of Davis et al (figure 6B, the authentication and verification functions of Davis correspond to the applicant's comparison of reconverted hash to image hash (signature)) suggest such limitations.

Conclusion

27. Any inquiry concerning this communication or earlier communications from examiner should be directed to Ronald Baum, whose telephone number is (703) 305-4276. The examiner can normally be reached Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Vu, can be reached at (703) 305-4393. The Fax number for the organization where this application is assigned is 703-872-9306.

Ronald Baum

Patent Examiner

KIM VU
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